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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/651,458	08/29/2003	Shunpei Yamazaki	0553-0164.01	8760

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EXAMINER	
LE, THAO X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 03/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/651,458	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Thao X. Le	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/517,542.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claim 42 is rejected under 35 U.S.C. 102(e) as being anticipated by US 6157429 to Miyawaki et al.

Regarding claim 42, Miyawaki discloses a display device in fig. 3 comprising: a silicon substrate 1, an insulating layer 6 formed on the silicon substrate 1; a field effect transistor 4 formed on the insulating layer 6; an interlayer insulating film 9 formed over the filed effect transistor 4; an EL element 14 formed on the interlayer insulating film 9, the EL element 12/14/15 comprising a pair of electrodes 15/12, column 13 line 47, and an EL layer interposed therebetween, wherein one of the pair of electrodes 12 is electrically connected to the field effect transistor 4, fig. 3.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 18-41 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6157429 to Miyawaki et al. in view of US 6583057 to Alluri et al. and US 4839707 to Shields

Regarding claims 18, 19, Miyawaki discloses a display device in fig. 3 or 11H comprising: a silicon substrate 1 (201), column 12 line 26, a field effect transistor, column 12 line 28, a gate electrode 4 (205), column 12 line 27, adjacent to the semiconductor substrate 1 with a gate insulating film 6 (204), column 10 lines 35-37 (the formation of insulating layer and FET can also be seen in fig. 11a-11h) interposed therebetween, a dielectric film 8 comprising PSG, column 12 line 56 and column 13 line 17, formed over the field effect transistor 4, a light shielding layer 7, column 12 line 62, formed over the dielectric film 8; a dielectric layer 9, column 13 line 27, formed on the

light shielding layer 7; and a pixel electrode 12', column 12 line 60, formed on the dielectric layer 9.

But, Miyawaki does not expressly disclose a the device comprising a insulating layer formed on the silicon substrate wherein a field effect transistor comprising a semiconductor layer formed on an upper surface of the insulating layer (a SOI substrate) and the resin film at least one selected from the group consisting of polyimide over the field effect transistor.

However, Alluri reference discloses the dielectric layer 210 in fig. 6 comprises PSG or polyimide resin, column 2 lines 35-40. At the time of the invention was made; it would have been obvious to one of ordinary skill in the art to replace the PSG layer 8 of Miyawaki with polyimide resin layer teaching of Alluri, because such material substitution would have been considered a mere substitution of art-recognized equivalent values, MPEP 2144.06.

With respect to SOI substrate, Shields discloses a display device in fig. 1 comprising a semiconductor layer 15, column 4 line 18, formed on an upper surface of the insulating layer 13 column 4 line 18, and a gate electrode 29, column 45 line 34, adjacent to the semiconductor layer 15 with a gate insulating 27, column 4 line 34, interposed therebetween (SOI substrate). At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the SOI teaching of Shields with display device of Miyawaki, because the SOI structure would have isolated both the polysilicon layer and the device layer

that would have eliminated shorts rising from leaky diodes as taught by Shields, column 3 line 55-60.

Regarding claims 20, 26, 32, 38, Miyawaki discloses the display device wherein the light shielding layer 7 comprises at least one selected from the group consisting of aluminum, titanium, and tantalum, column 12 line 64.

Regarding claims 21-22, 27-28, 33-34, and 39-40, Miyawaki disclose a display device wherein the dielectric layer 9 comprises at least one selected from the group consisting of silicon oxide, silicon nitride, silicon oxynitride, DLC (Diamond like carbon), and polyimide, column 8 line 17, wherein the pixel electrode 12' comprises aluminum, column 8 line 8.

Regarding 23, 28, 35, 41, and 43, Miyawaki does not disclose a display device wherein the display device is one selected from the group consisting of a portable telephone, a video camera, a mobile computer, a goggle type display, a projector, an electronic book, a digital camera, and a DVD player. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the teaching of Miyawaki as claimed for intended used, MPEP 2144.07.

Regarding claims 24-25, Miyawaki discloses a display device in fig. 3 or 11H comprising: a silicon substrate 1 (201), a field effect transistor comprising a gate electrode 4 (205) adjacent to the semiconductor substrate 1 (201) with a gate insulating film 6 (204) interposed therebetween; a PSG dielectric film 8, column 12 line 56, formed over the field effect transistor, a light shielding layer 7, column 12 line 62, formed over the dielectric film 8; a dielectric layer 9, column 13 line 27, formed on the light shielding

layer 7; and a pixel electrode 12', column 12 line 60, formed on the dielectric layer 9, wherein a storage capacitance is formed by the light shielding layer 7, the dielectric layer 9, and the pixel electrode 12', column 13 line 25.

But, Miyawaki does not expressly disclose the device comprising an insulating layer formed on the silicon substrate a filed effect transistor comprising a semiconductor layer formed on an upper surface of the insulating layer (SOI substrate), and the resin film at least one selected from the group consisting of polyimide over the field effect transistor.

However, Alluri reference discloses the dielectric layer 210 in fig. 6 comprises PSG or polyimide resin, column 2 lines 35-40. At the time of the invention was made; it would have been obvious to one of ordinary skill in the art to replace the PSG layer of Miyawaki with polyimide layer use the polyimide dielectric layer teaching of Alluri, because such material substitution would have been considered a mere substitution of art-recognized equivalent values, MPEP 2144.06.

With respect to SOI substrate, Shields discloses a display device in fig. 1 comprising a semiconductor layer 15, column 4 line 18, formed on an upper surface of the insulating layer 13 column 4 line 18, and a gate electrode 29, column 45 line 34, adjacent to the semiconductor layer 15 with a gate insulating 27, column 4 line 34, interposed therebetween (SOI substrate). At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the SOI teaching of Shields with display device of Miyawaki, because the

SOI structure would have isolated both the polysilicon layer and the device layer that would have eliminated shorts rising from leaky diodes as taught by Shields, column 3 line 55-60.

Regarding claims 30-31, Miyawaki discloses a display device in fig. 3 comprising: a pair of substrates 1/16, column 13 line 46 wherein one of the pair of substrates comprises a silicon substrate 1, and a liquid crystal material 14, column 13 line 36, is interposed between the pair of substrates 1/16, fig. 3, a field effect transistor comprising a gate electrode 4 (205) adjacent to the semiconductor substrate 1 with a gate insulating film 6 (204) interposed therebetween; a PSG dielectric film 8, column 12 line 56, formed over the field effect transistor, a light shielding layer 7, column 12 line 62, formed over the dielectric film; a dielectric layer 9, column 13 line 27, formed on the light shielding layer; and a pixel electrode 12', column 12 line 60, formed on the dielectric layer, wherein a storage capacitance is formed by the light shielding layer 7, the dielectric layer 9, and the pixel electrode 12', column 13 line 25.

But, But, Miyawaki does not expressly disclose the device comprising an insulating layer formed on the silicon substrate a filed effect transistor comprising a semiconductor layer formed on an upper surface of the insulating layer (SOI substrate), and the resin film at least one selected from the group consisting of polyimide over the field effect transistor.

However, Alluri reference discloses the dielectric layer 210 in fig. 6 comprises PSG or polyimide resin, column 2 lines 35-40. At the time of the invention was made; it would have been obvious to one of ordinary skill in the art

to replace the PSG layer of Miyawaki with polyimide layer use the polyimide dielectric layer teaching of Alluri, because such material substitution would have been considered a mere substitution of art-recognized equivalent values, MPEP 2144.06.

With respect to SOI substrate, Shields discloses a display device in fig. 1 comprising a semiconductor layer 15, column 4 line 18, formed on an upper surface of the insulating layer 13 column 4 line 18, and a gate electrode 29, column 45 line 34, adjacent to the semiconductor layer 15 with a gate insulating 27, column 4 line 34, interposed therebetween (SOI substrate). At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the SOI teaching of Shields with display device of Miyawaki, because the SOI structure would have isolated both the polysilicon layer and the device layer that would have eliminated shorts rising from leaky diodes as taught by Shields, column 3 line 55-60.

Regarding claims 36-37, see discussion in the above claims 18-19 and 30-31

Response to Arguments

6. Applicant's arguments with respect to claims 18-41have been considered but are moot in view of the new ground(s) of rejection.

7. With respect to claim 42, the Applicant's arguments filed 27 Jan 2005 have been fully considered but they are not persuasive. The Applicant argues that Miyawaki does not disclose or suggest the display device. The Examiner respectfully disagree because

Miyawaki clearly shows that the invention is a display device, see filed of invention and fig. 3. Furthermore, the recitation 'a display device' s not been given patentable weight because it have been held that a preamble is denied the effect of a limitation where the claim is drawn to a structure and the portion of the claim following the preamble is a self-contained description of the structure not depending for completeness upon the introductory clause. Kropa v. Robie, 88 USPQ 478 (CCPA 1951)

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thao X. Le
24 Feb. 2005

LONG PHAM
PRIMARY EXAMINER